This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF THE CLAIMS:**

Claim 1 (Currently Amended) A DRAM device comprising:

a deep trench capacitor formed in a semiconductor substrate for receiving and storing a voltage;

a storage cell including a vertical pass transistor having source and drain regions formed in a p-well, said drain region formed by a diffusion in said p- well outside said deep trench capacitor adjacent ~~said~~ a first buried strap to conduct said voltage to said trench capacitor; and

a control cell for controlling the threshold voltage of the vertical pass transistor according to a voltage of a gate connecting a second buried strap and diffusion region formed in the p-well region, said second buried strap region and diffusion region formed in said p- well region of said control cell being at a lower depth than the first buried strap and diffusion region formed in said p- well region of said storage cell, wherein a voltage applied at a gate connecting said second buried strap and diffusion region controls said threshold voltage of the vertical pass transistor in accordance with a depletion region formed in said p- well region by application of said applied gate voltage.

Claim 2 (Currently Amended) The DRAM device according to Claim 1, wherein ~~a voltage of a gate connecting a second buried strap and diffusion region further controls the conductive state of the vertical pass transistor,~~ said gate voltage ~~comprising~~ comprises a wordline (WL) voltage controlling access to data stored in said deep trench capacitor via said vertical pass transistor.

Claim 3 (Canceled)

Claim 4 (Currently Amended) The DRAM device according to Claim [[3]] 2, wherein said depletion region formed at said second buried strap and diffusion region pinches off the p-well to disconnect the p-well region into two regions, a first conductive and second floating p-well

region, wherein the floating p-well region enables a lower threshold voltage for turning on said vertical pass transistor during WL active state.

Claim 5 (Currently Amended) The DRAM device according to Claim [[3]] 2, wherein said depletion region formed at said second buried strap and diffusion region does not pinch off the p-well at WL inactive state.

Claim 6 (Original) The DRAM device according to Claim 1, wherein a bitline voltage to be stored in said DRAM cell in a write operation is connected with a source of said vertical pass transistor.

Claim 7 (Original) The DRAM device according to Claim 1, wherein said drain of said vertical pass transistor is formed by a diffusion at said first buried strap.

Claim 8 (Original) The DRAM device according to Claim 1, wherein a gate at storage cell and control cell share the same wordline, the threshold voltage of the storage cell being modified according to the voltage at said wordline.

Claims 9 – 14 (Canceled)

Claim 15 (Original) A method of improving performance of a DRAM cell comprising:

a) providing two deep trenches, one trench including a vertical storage cell and deep trench capacitor for storing data and a second trench including a vertical control cell for controlling voltage at a p-well region separating the vertical storage and control cells;

b) applying a voltage to a common conductor connecting a gate of each said vertical storage and control cell, said voltage being of a value enabling pinch-off of said p-well structure to thereby render said p-well region into a p-well floating condition having a first floating region and a second conductive region, wherein said p-well floating condition decreases the threshold voltage

of said vertical storage cell when in an on-state as compared to when in an off-state thus resulting in increased gate over-drive and drive current.

Claim 16 (Original) The method as claimed in Claim 15, wherein said common conductor is a wordline having a wordline active or inactive voltage state, said step b) of applying a voltage to a common conductor including: applying a wordline active voltage to enable reduction of storage cell gate threshold voltage to thereby increase drive current, or applying a wordline inactive voltage to turn off said storage cell, said wordline voltages being simultaneously applied to both gates of the storage and control cells.

Claim 17 (Original) The method as claimed in Claim 15, wherein a vertical storage cell for storing data includes a vertical pass transistor having a drain diffusion region formed in the p-well at a first buried strap location connecting said trench capacitor and, said vertical control cell includes a second diffusion region formed in the p-well at a second buried strap location for controlling conductive state of said vertical pass transistor.

Claim 18 (Original) The method as claimed in Claim 17, wherein said second diffusion region formed in the p-well at a second buried strap location is lower in depth than the drain diffusion region formed in the p-well at a first buried strap location.

Claims 19 – 20 (Canceled)